

What is claimed is:

- 1        1. In circuitry, protection from the effects of spike and surge over voltage occurrences,  
2           comprising:  
3              an element positioned between a node in said circuitry and a reference voltage,  
4              said element having a body of dielectric material with first and second essentially  
5              parallel faces separated by a thickness dimension and having conductive  
6              contact over each of said first and said second faces,  
7              said body of dielectric material having a property that;  
8              in the presence of an increasing field between said contacts over said first and  
9              said second faces, there is an increase in current flow at a first rate, and  
10             in the presence of a field in the vicinity of 2Mv/cm and above, there is a  
11             a nondestructive unlimited current flow second rate, and,  
12             means connecting said conductive contact on said first face of said body to said node in  
13             said circuitry, and,  
14             means connecting said conductive contact on said second face of said body to said  
15             reference voltage.
- 1        2. The over voltage protection of claim 1 wherein said body of dielectric material is an  
2           amorphous alloy member having a thickness in the sub 200 nanometer range.
- 1        3. The over voltage protection of claim 2 wherein the thickness of said body of  
2           dielectric material is about 50 nanometers.

1       4. The over voltage protection of claim 1 wherein said body of dielectric material is a  
2       deposited amorphous alloy taken from the group comprising amorphous hydrogenated  
3       silicon carbide ( SiCH), carbon doped oxides, SiCOH, amorphous hydrogenated  
4       carbon, diamond like carbon (DLC), and fluorinated diamond like carbon (FDLC).

1       5 The method of providing over voltage protection in an integrated circuit,  
2       comprising the steps of:  
3       positioning a body of dielectric material between a node in said integrated circuit and  
4                          ground,  
5       said body having first and second essentially parallel surfaces separated by  
6                          a thickness dimension with a conductive contact over each of said first  
7                          and said second surfaces,  
8       said body, in the presence of an increasing field between said contacts  
9                          over said first and said second faces, exhibiting an increase in current  
10                         flow at a first rate, and in the presence of a field in the vicinity of  
11                         2Mv/cm and above, exhibiting a nondestructive breakdown type  
12                         unlimited current flow second rate, and,  
13       connecting said conductive contact on said first face of said body to said node in  
14                         said circuitry, and,  
15       connecting said conductive contact on said second face of said body to said ground.

1       6. The method of claim 5 wherein said positioning of said body is by deposition to a  
2                   thickness in the sub 200 nanometer range.

1       7. The method of claim 6 wherein said deposition is 50 nanometers thick.

1       8. The method of claim 5 wherein said deposition is of an amorphous alloy taken from  
2                   the group comprising amorphous hydrogenated silicon carbide ( SiCH), carbon doped  
3                   oxides, SiCOH, amorphous hydrogenated carbon, diamond like carbon (DLC), and  
4                   florinated diamond like carbon (FDLC).

1       9. An overvoltage protection member for use in circuitry in which over voltage spikes  
2                   and surges may occur comprising in combination :  
3                   a body of dielectric material between a node in said integrated circuit and ground,  
4                   said body having first and second essentially parallel surfaces separated by  
5                   a thickness dimension with a metal layer over each of said first  
6                   and said second surfaces,  
7                   said body, in the presence of an increasing field between said contacts  
8                   over said first and said second faces, passing increasing current at a  
9                   first flow rate, and in the presence of a selected field,  
10                  passing current at an unlimited second flow rate, and,  
11                  said metal layer on said first surface of said body being connected to said node in  
12                  said circuitry, and,  
13                  said metal layer on said second surface of said body being connected to ground.

1       10. The protection member of claim 9 wherein said selected field is in the vicinity of  
2           2Mv/cm,

1       11. The protection member of claim 9 wherein said dielectric material is an amorphous  
2       alloy taken from the group comprising amorphous hydrogenated silicon carbide ( SiCH),  
3       carbon doped oxides, SiCOH, amorphous hydrogenated carbon, diamond like carbon  
4       (DLC), and fluorinated diamond like carbon (FDLC).

1       12. The protection member of claim 11 wherein said thickness dimension is  
2           50 nanometers.

1       13. The protection member of claim 12 wherein said dielectric material is  
2           in deposited amorphous form.

1       14. The method of fabricating an over voltage protection member in an integrated  
2       circuit member,  
3       comprising the steps of:  
4       providing a layer of amorphous alloy material in said integrated circuit member,  
5       said layer of amorphous alloy being of a thickness that permits voltage at the  
6       magnitude of said over voltage to be passed, and,  
7       for each circuit node in said integrated circuit for which over voltage protection  
8       is desired,

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9 providing on a first side of said amorphous alloy layer, a specific protection area contact  
10 connected to said circuit node, and,  
11 providing high conductivity path means to reference potential,  
12 at the second and opposite side of said amorphous alloy layer at said circuit node  
13 location.

1        15. The method of claim 14 wherein in said step of providing an amorphous alloy layer  
2              the material of said layer is taken from the group comprising amorphous hydrogenated  
3              silicon carbide ( SiCH), carbon doped oxides, SiCOH, amorphous hydrogenated  
4              carbon, diamond like carbon (DLC), and fluorinated diamond like carbon (FDLC).

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